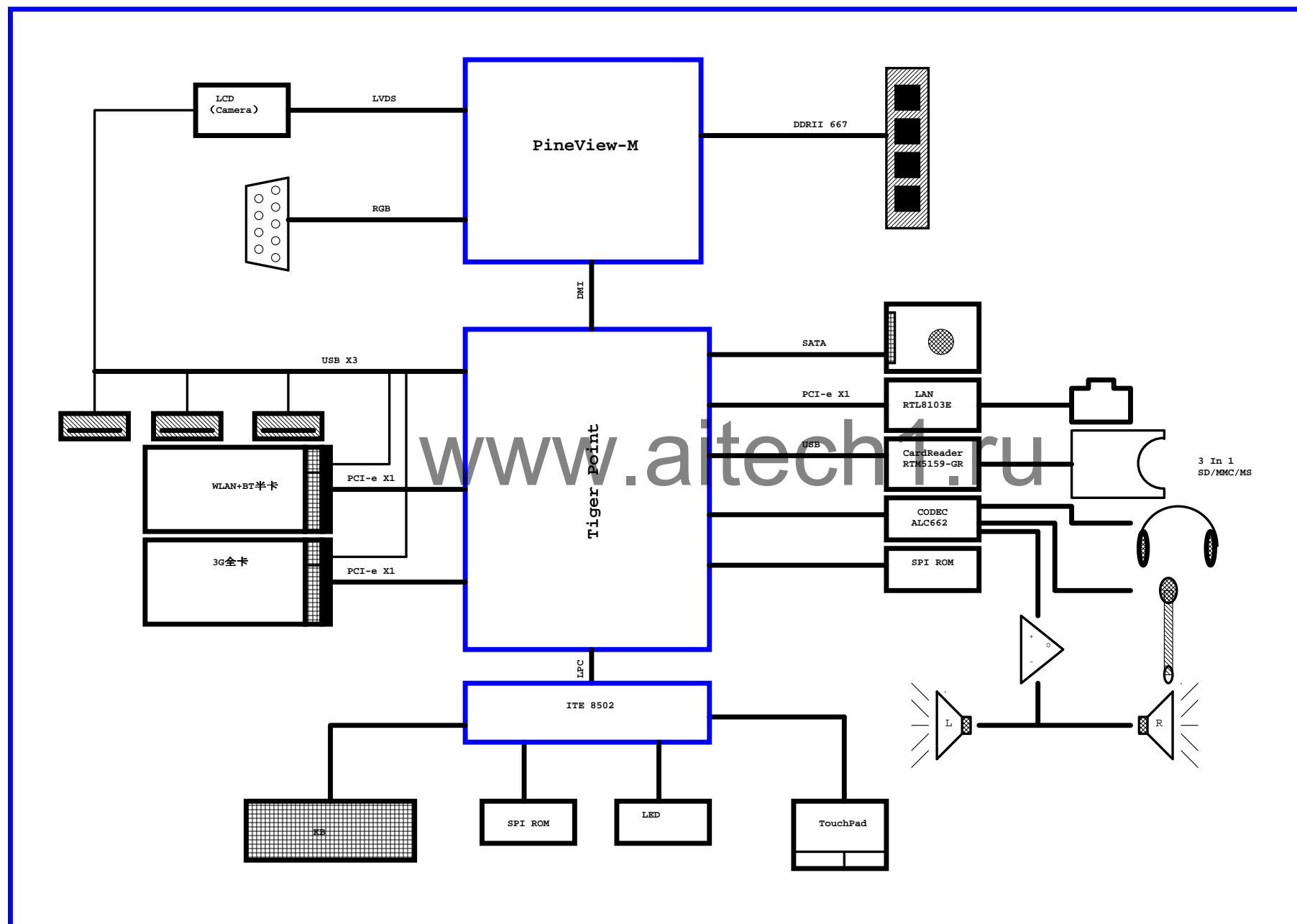
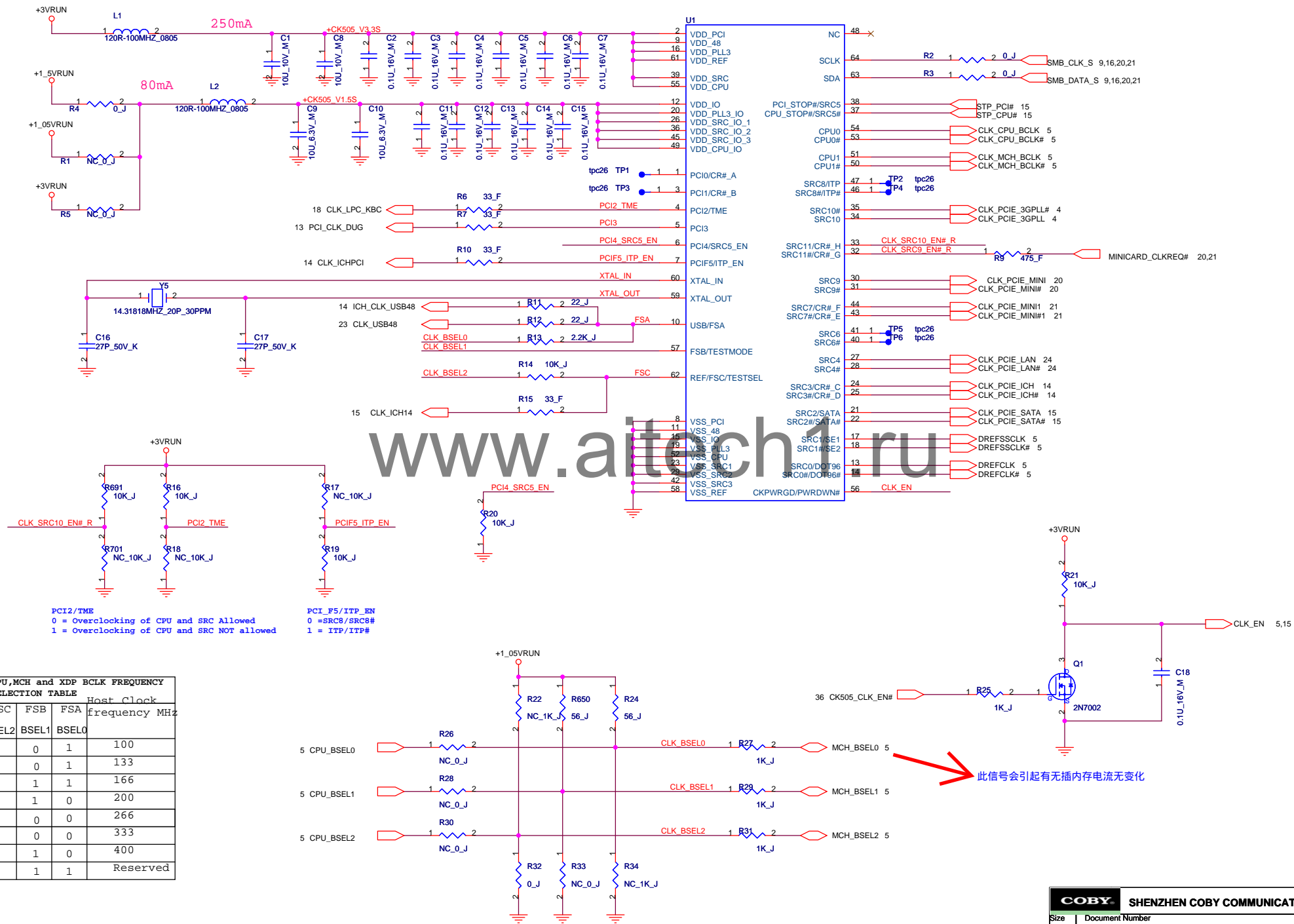
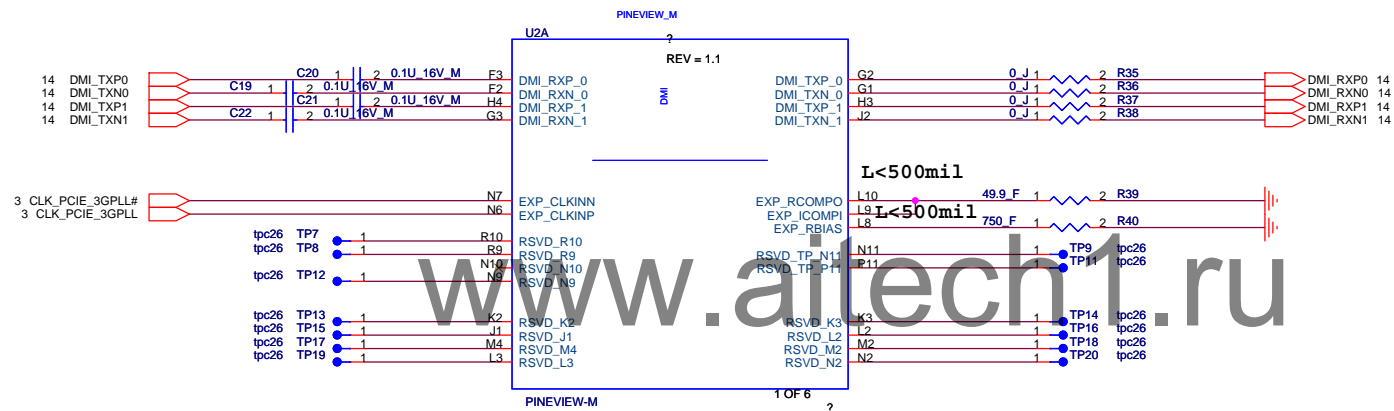
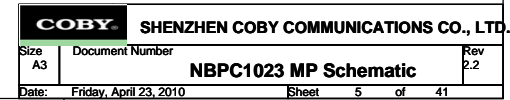


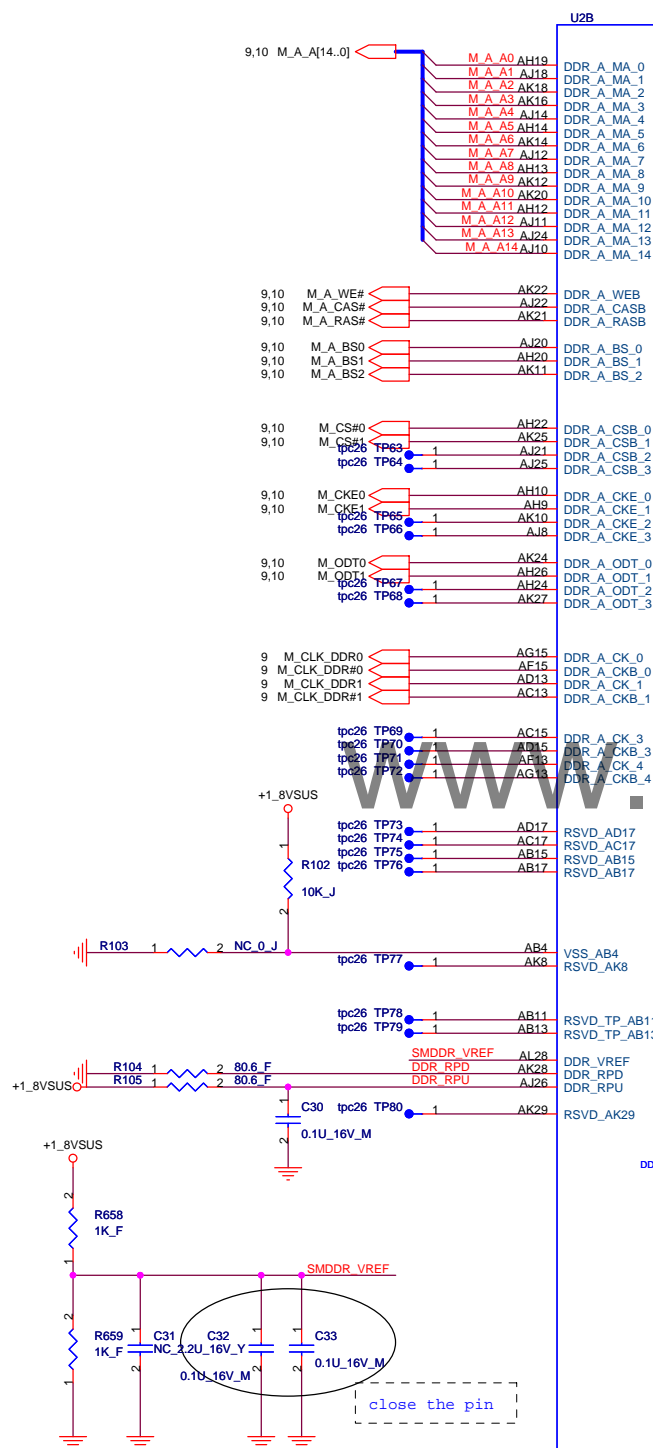
COBY NBPC1023 System Block Diagram











PINEVIEW_M

REV = 1.1

PINEVIEW-M

DDR_A_DQS_0 → AD3 M A DQS0
DDR_A_DQS#0 → AD2 M A DQS#0
DDR_A_DM_0 → AD4 M A DM0

DDR_A_DQ_0 → AC4 M A DQ0
DDR_A_DQ_1 → AC1 M A DQ1
DDR_A_DQ_2 → AE4 M A DQ2
DDR_A_DQ_3 → AG2 M A DQ3
DDR_A_DQ_4 → AB2 M A DQ4
DDR_A_DQ_5 → AB3 M A DQ5
DDR_A_DQ_6 → AE2 M A DQ6
DDR_A_DQ_7 → AE3 M A DQ7

DDR_A_DQS_1 → AB8 M A DQS1
DDR_A_DQS#1 → AD7 M A DQS#1
DDR_A_DM_1 → AA9 M A DM1

DDR_A_DQ_8 → AB6 M A DQ8
DDR_A_DQ_9 → AB7 M A DQ9
DDR_A_DQ_10 → AE5 M A DQ10
DDR_A_DQ_11 → AG5 M A DQ11
DDR_A_DQ_12 → AA5 M A DQ12
DDR_A_DQ_13 → AB5 M A DQ13
DDR_A_DQ_14 → AB9 M A DQ14
DDR_A_DQ_15 → AD6 M A DQ15

DDR_A_DQS_2 → AD8 M A DQS2
DDR_A_DQS#2 → AD10 M A DQS#2
DDR_A_DM_2 → AE8 M A DM2

DDR_A_DQ_16 → AG8 M A DQ16
DDR_A_DQ_17 → AG7 M A DQ17
DDR_A_DQ_18 → AE10 M A DQ18
DDR_A_DQ_19 → AG11 M A DQ19
DDR_A_DQ_20 → AE7 M A DQ20
DDR_A_DQ_21 → AE8 M A DQ21
DDR_A_DQ_22 → AD11 M A DQ22
DDR_A_DQ_23 → AE10 M A DQ23

DDR_A_DQS_3 → AK5 M A DQS3
DDR_A_DQS#3 → AK3 M A DQS#3
DDR_A_DM_3 → AJ3 M A DM3

DDR_A_DQ_24 → AH1 M A DQ24
DDR_A_DQ_25 → AJ2 M A DQ25
DDR_A_DQ_26 → AK6 M A DQ26
DDR_A_DQ_27 → AJ7 M A DQ27
DDR_A_DQ_28 → AF3 M A DQ28
DDR_A_DQ_29 → AH2 M A DQ29
DDR_A_DQ_30 → AL5 M A DQ30
DDR_A_DQ_31 → AL6 M A DQ31

DDR_A_DQS_4 → AG22 M A DQS4
DDR_A_DQS#4 → AG21 M A DQS#4
DDR_A_DM_4 → AD19 M A DM4

DDR_A_DQ_32 → AE19 M A DQ32
DDR_A_DQ_33 → AG19 M A DQ33
DDR_A_DQ_34 → AF22 M A DQ34
DDR_A_DQ_35 → AD22 M A DQ35
DDR_A_DQ_36 → AG17 M A DQ36
DDR_A_DQ_37 → AE19 M A DQ37
DDR_A_DQ_38 → AE21 M A DQ38
DDR_A_DQ_39 → AD21 M A DQ39

DDR_A_DQS_5 → AE26 M A DQS5
DDR_A_DQS#5 → AG27 M A DQS#5
DDR_A_DM_5 → AJ27 M A DM5

DDR_A_DQ_40 → AE24 M A DQ40
DDR_A_DQ_41 → AG25 M A DQ41
DDR_A_DQ_42 → AD25 M A DQ42
DDR_A_DQ_43 → AD24 M A DQ43
DDR_A_DQ_44 → AC22 M A DQ44
DDR_A_DQ_45 → AG24 M A DQ45
DDR_A_DQ_46 → AD27 M A DQ46
DDR_A_DQ_47 → AE27 M A DQ47

DDR_A_DQS_6 → AE30 M A DQS6
DDR_A_DQS#6 → AF29 M A DQS#6
DDR_A_DM_6 → AE30 M A DM6

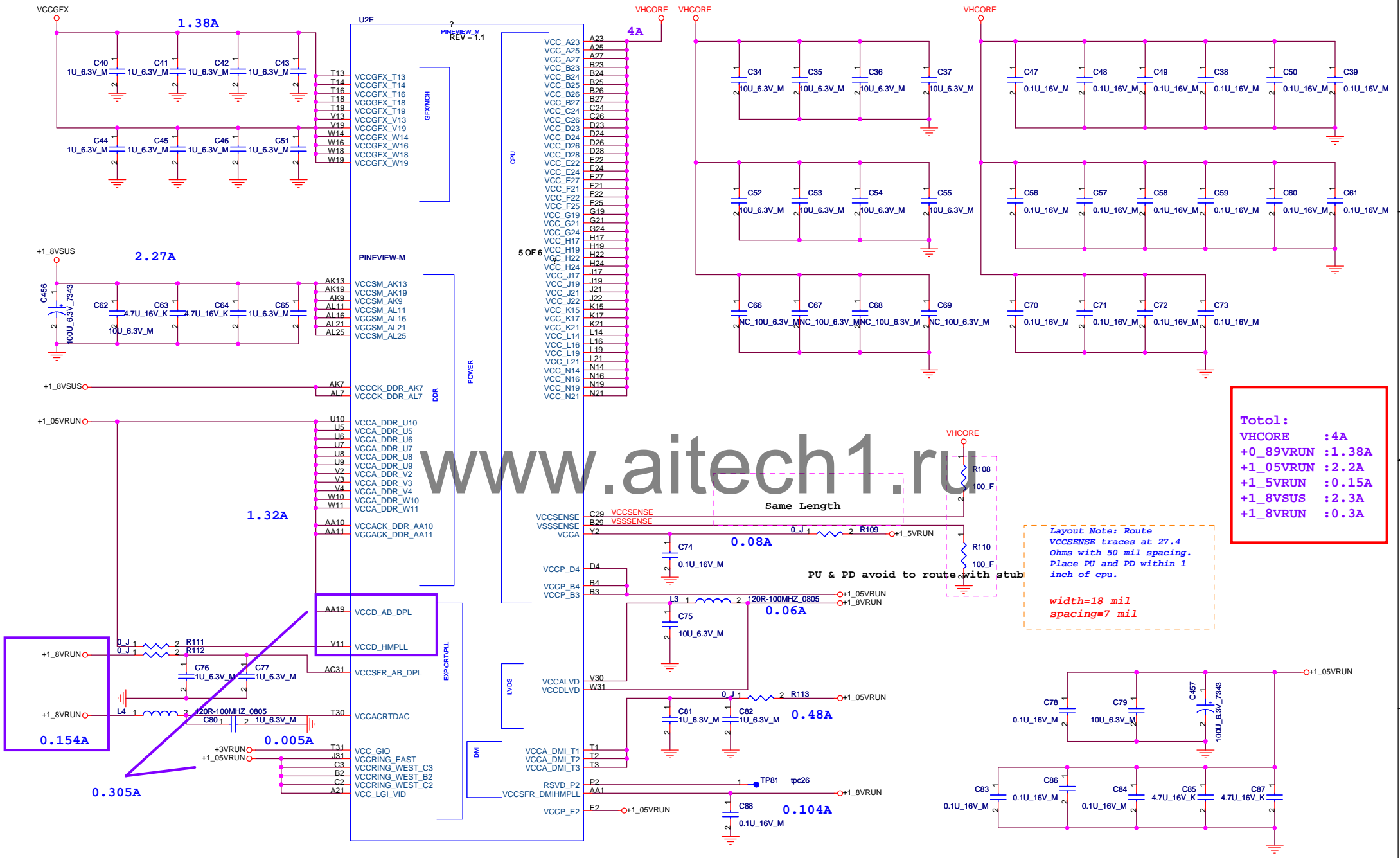
DDR_A_DQ_48 → AG31 M A DQ48
DDR_A_DQ_49 → AG30 M A DQ49
DDR_A_DQ_50 → AD30 M A DQ50
DDR_A_DQ_51 → AD29 M A DQ51
DDR_A_DQ_52 → AJ30 M A DQ52
DDR_A_DQ_53 → AJ29 M A DQ53
DDR_A_DQ_54 → AE29 M A DQ54
DDR_A_DQ_55 → AD28 M A DQ55

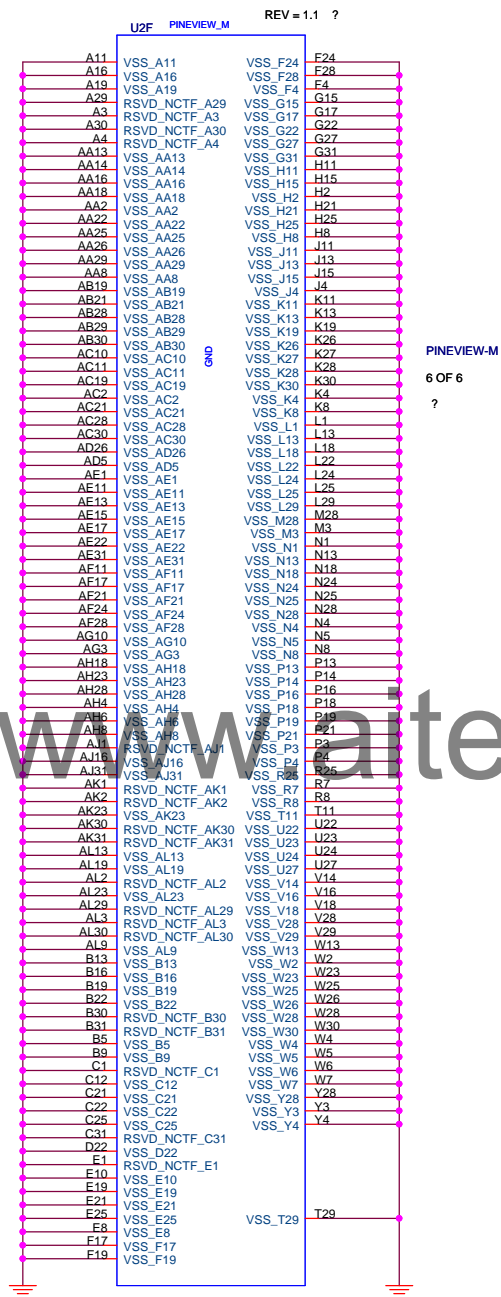
DDR_A_DQS_7 → AB27 M A DQS7
DDR_A_DQS#7 → AA27 M A DQS#7
DDR_A_DM_7 → AB26 M A DM7

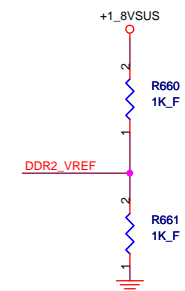
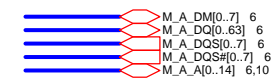
DDR_A_DQ_56 → AA24 M A DQ56
DDR_A_DQ_57 → AB25 M A DQ57
DDR_A_DQ_58 → W24 M A DQ58
DDR_A_DQ_59 → W22 M A DQ59
DDR_A_DQ_60 → AB24 M A DQ60
DDR_A_DQ_61 → AB23 M A DQ61
DDR_A_DQ_62 → AA23 M A DQ62
DDR_A_DQ_63 → W27 M A DQ63

M_A_DQ[63..0] 9
M_A_DQS#6[7..0] 9
M_A_DQS[7..0] 9
M_A_DM[7..0] 9

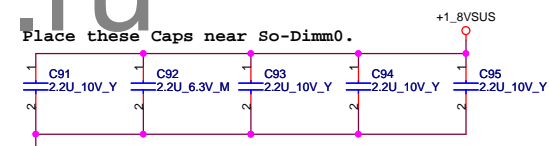
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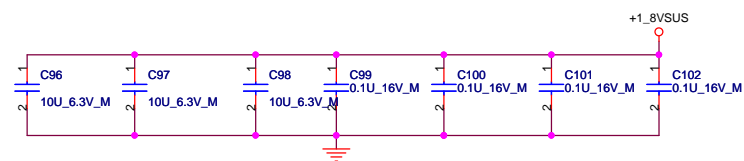


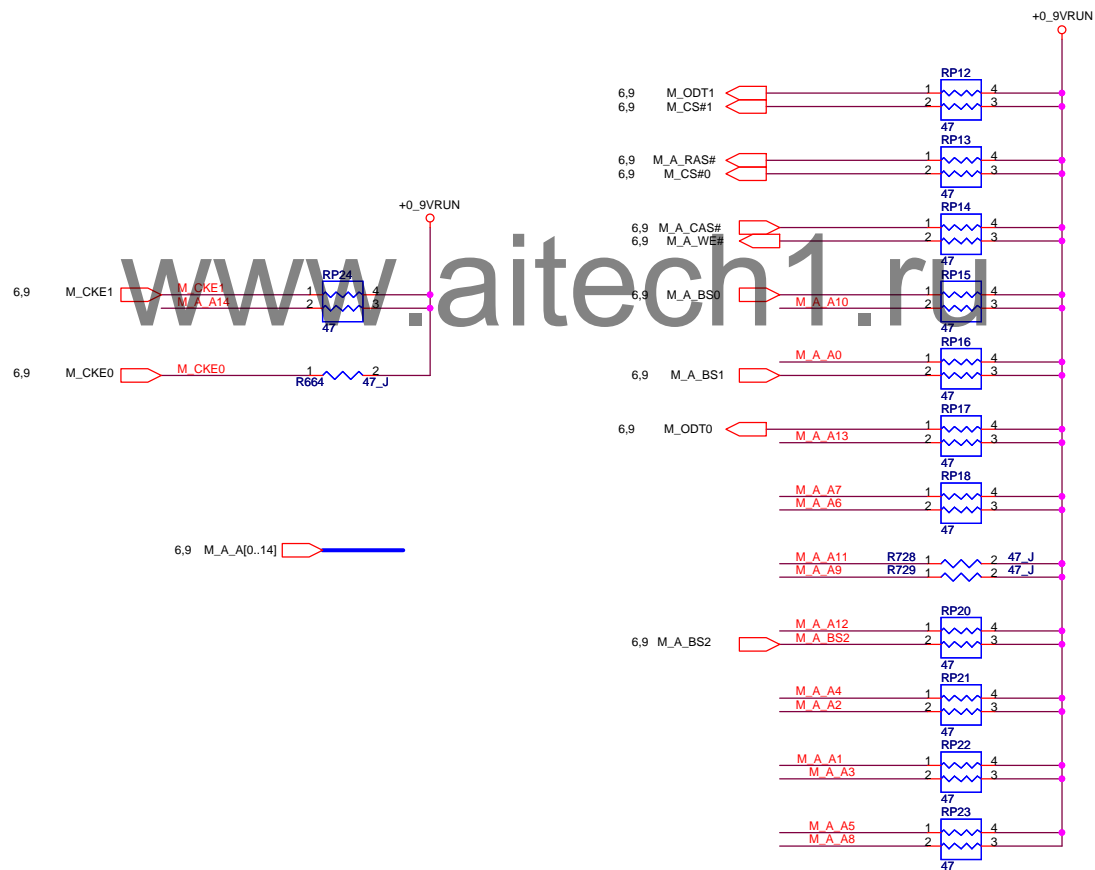
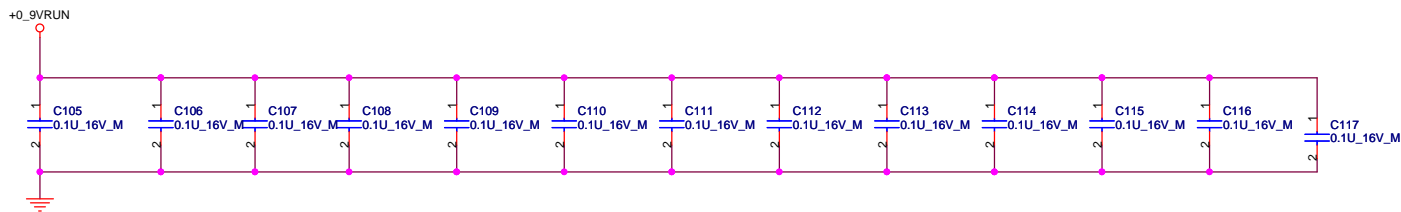


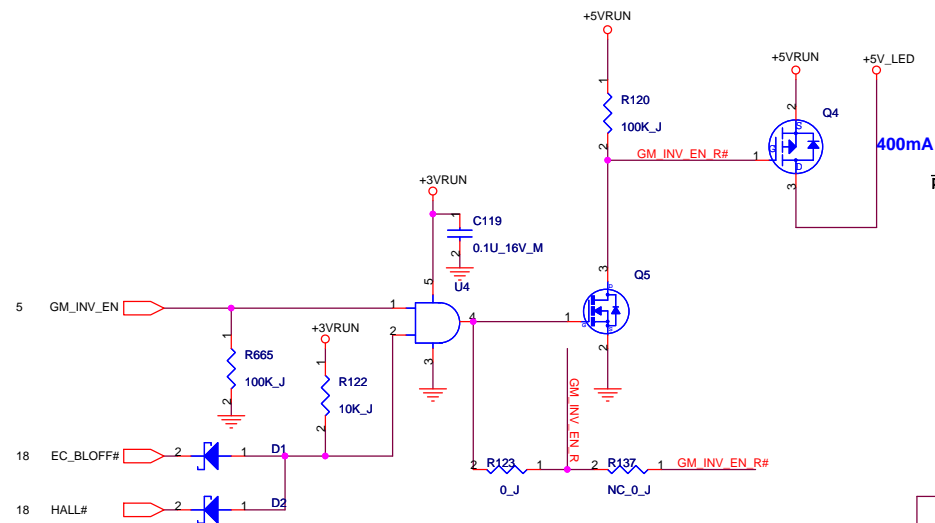
Place these Caps near So-Dimm0.



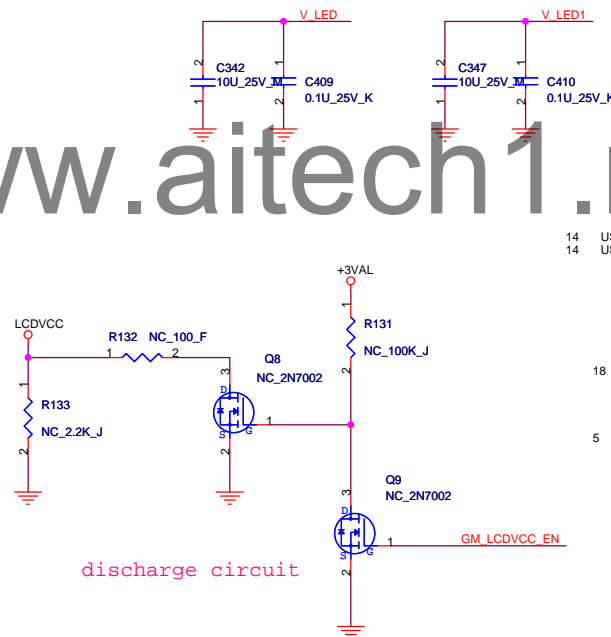
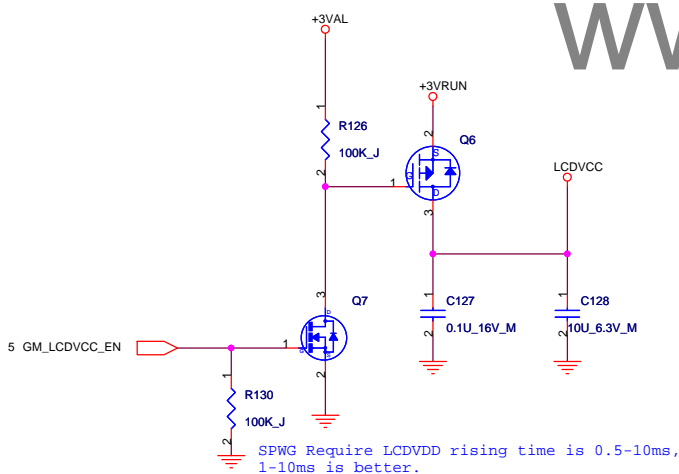
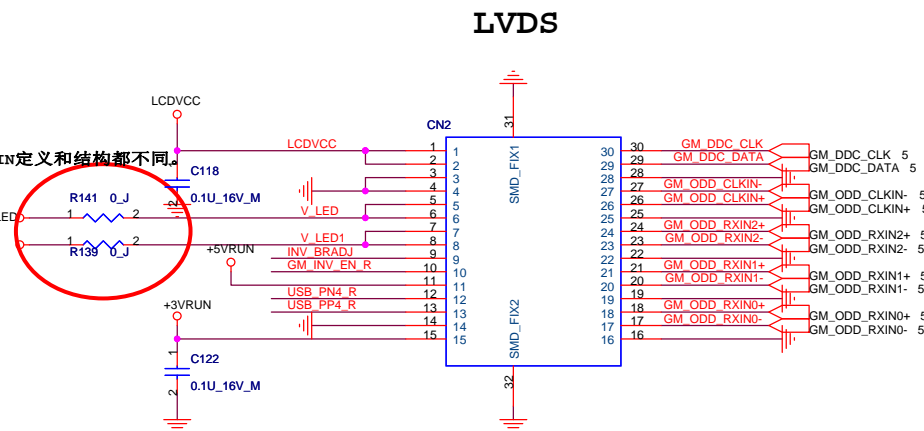
Place these Caps near So-Dimm0.



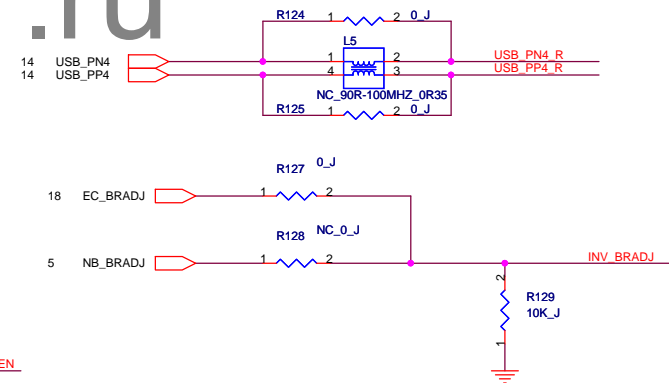




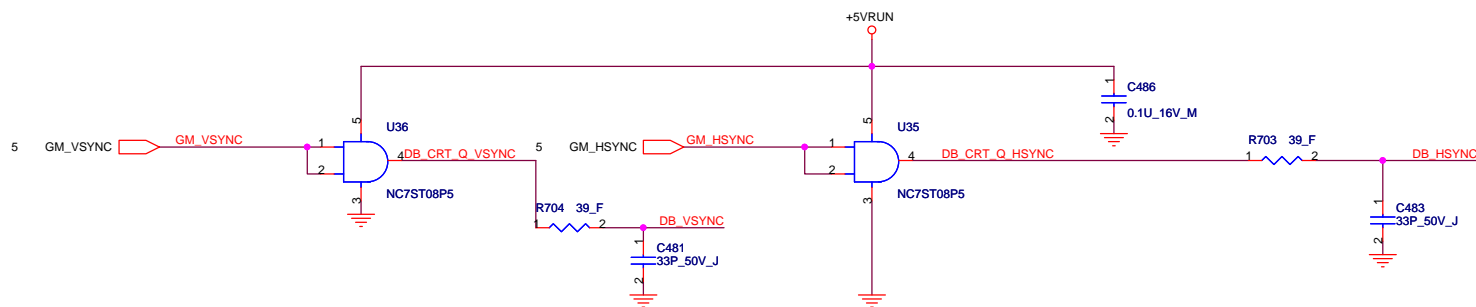
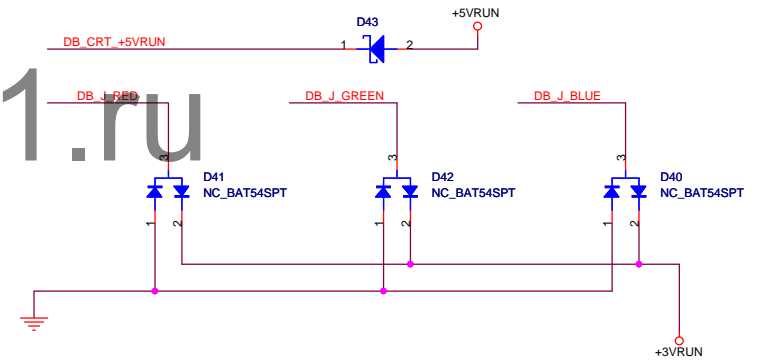
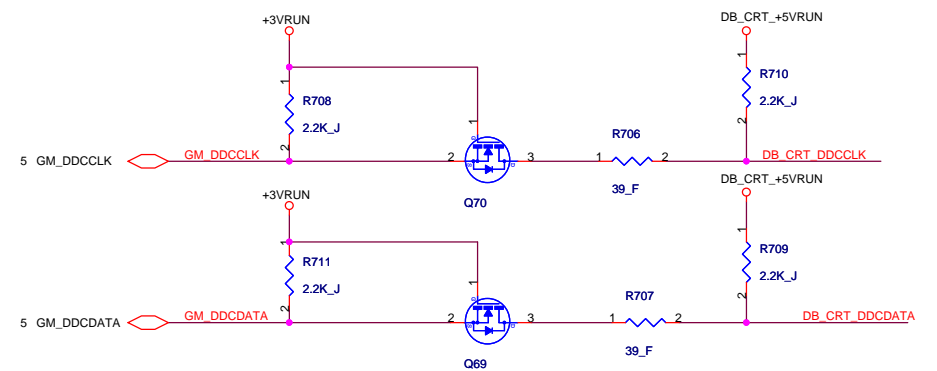
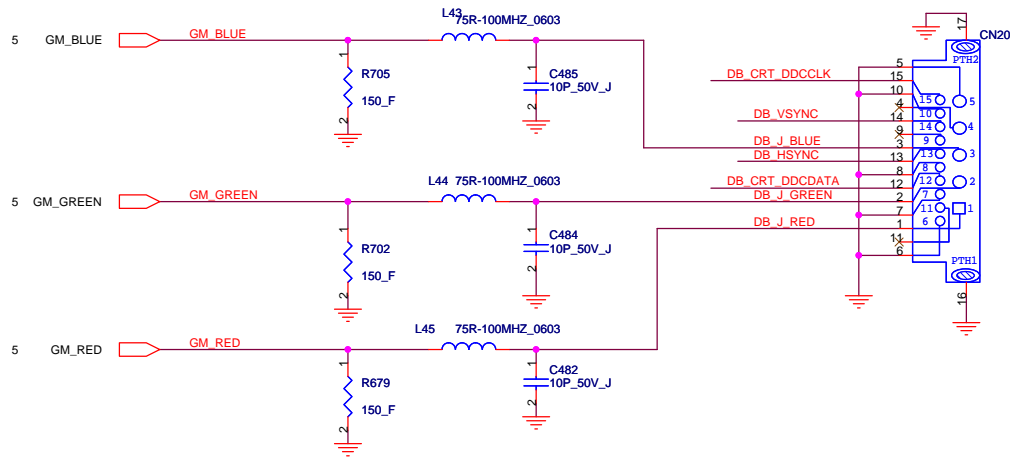
两种屏线PIN定义和结构都不同

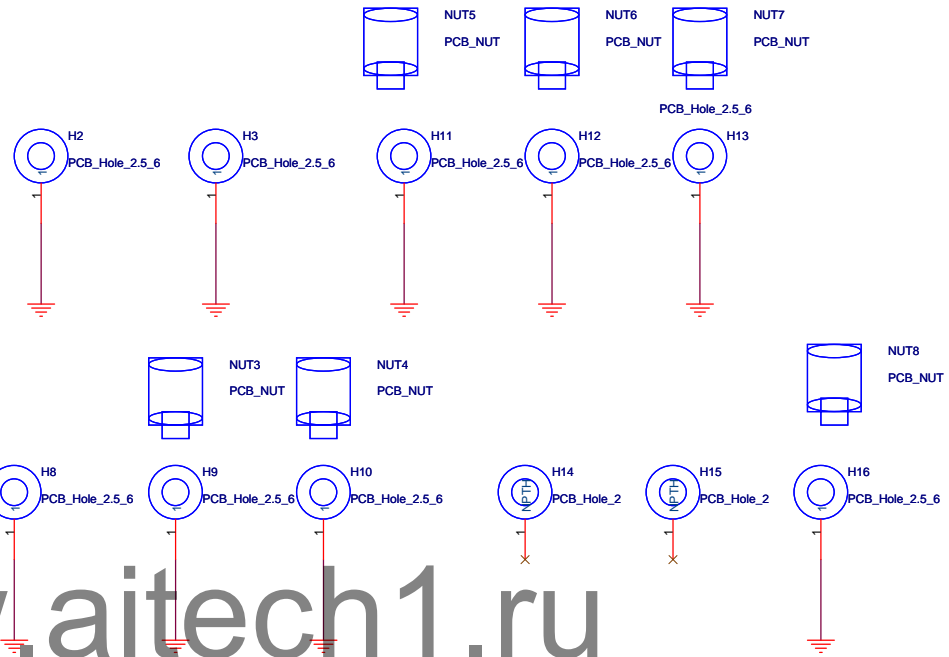
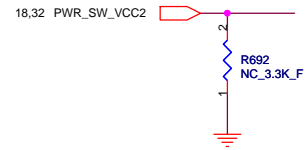


discharge circuit



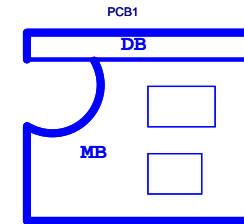
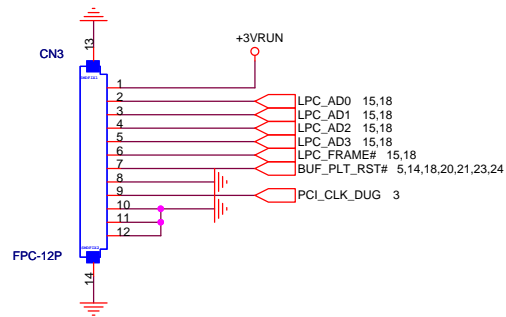
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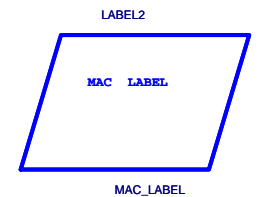
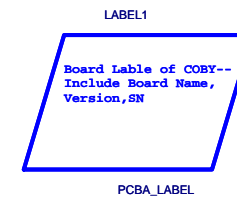


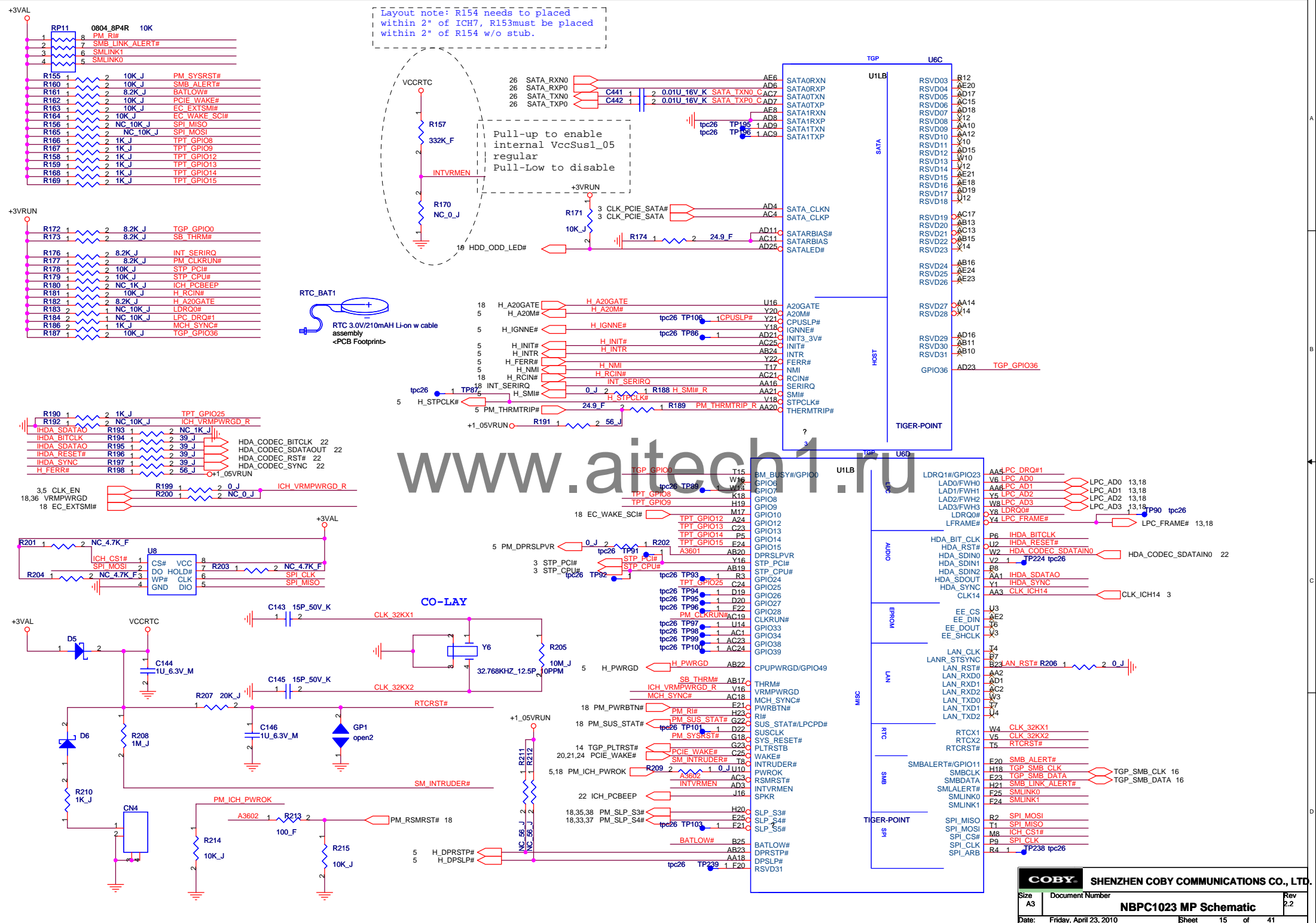
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DEBUG PORT



1028_PCB

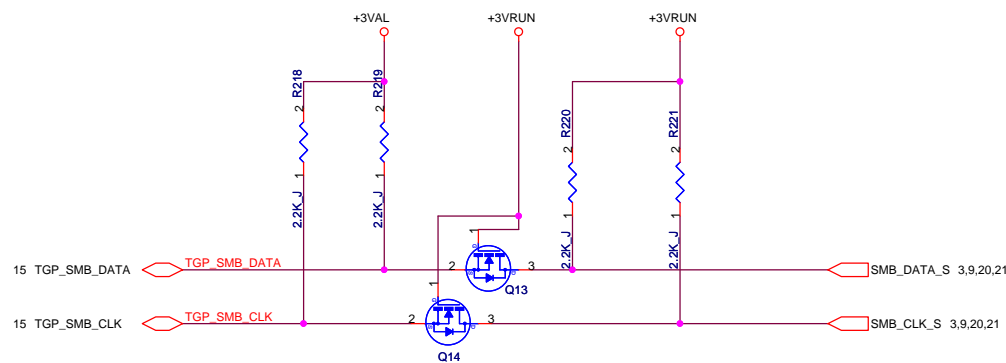


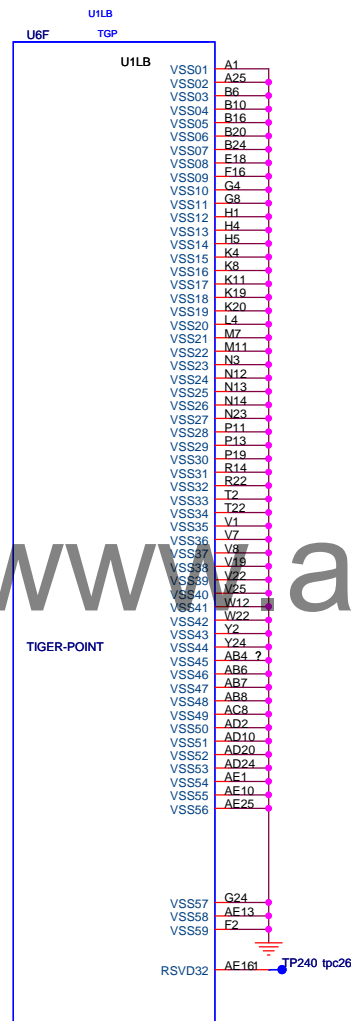


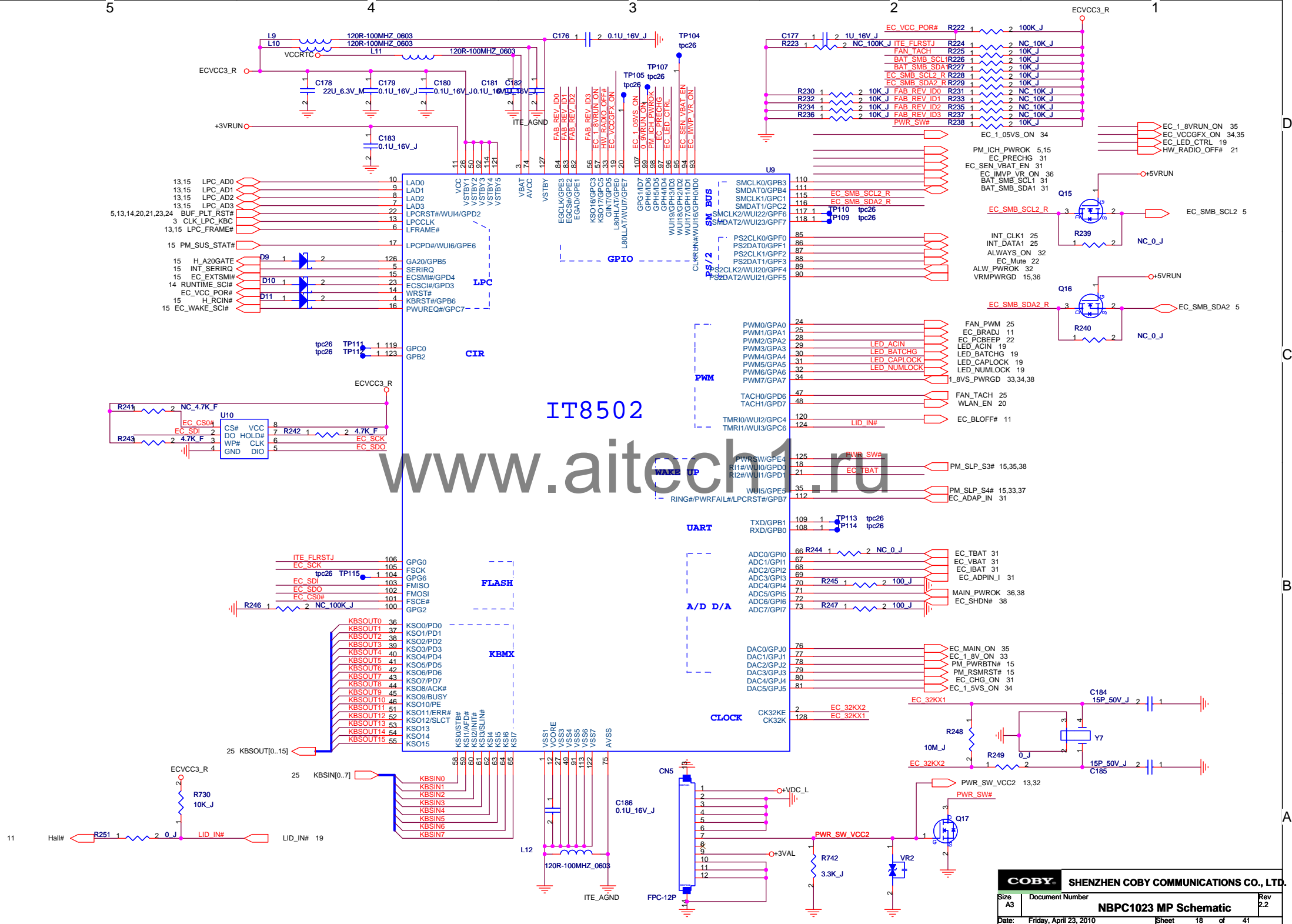
Layout note: R154 needs to be placed within 2" of ICH7, R153 must be placed within 2" of R154 w/o stub.

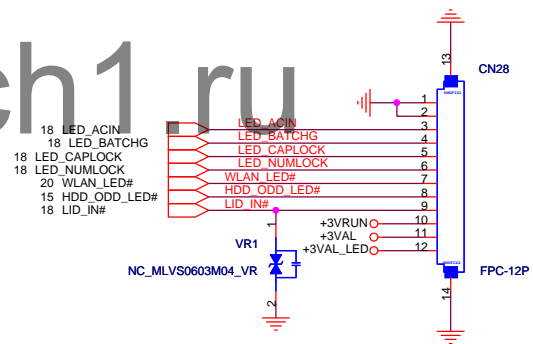
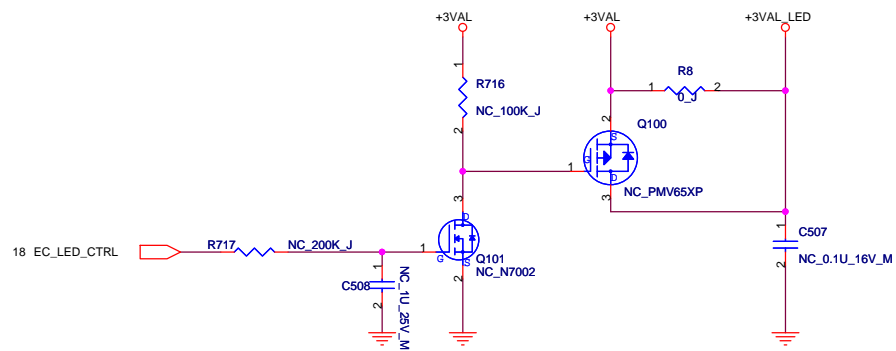
Pull-up to enable internal VccSus1_05 regular Pull-Low to disable

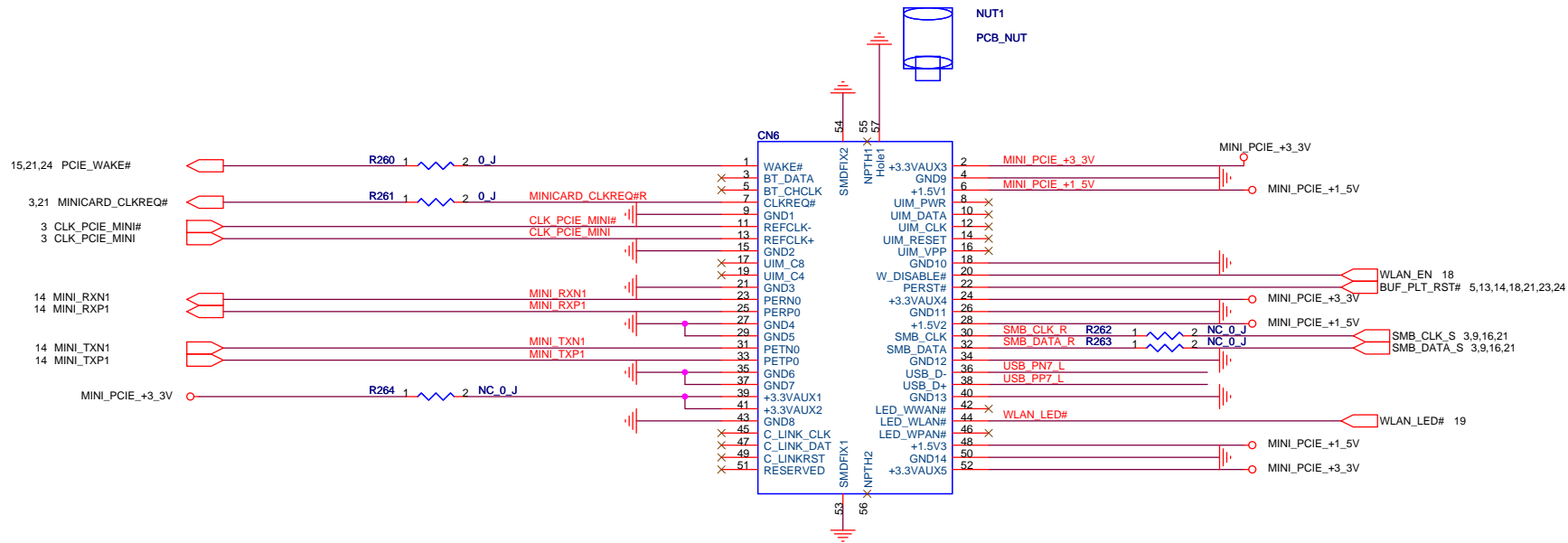
RTC_BAT1
RTC 3.0V/210mAh Li-on w cable assembly <PCB Footprint>



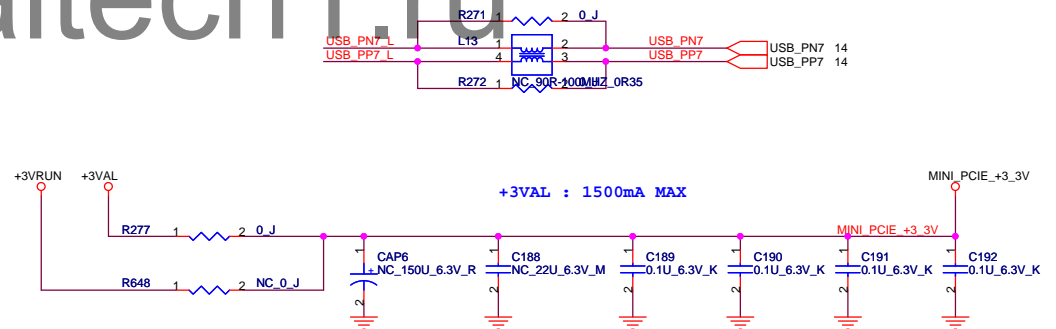
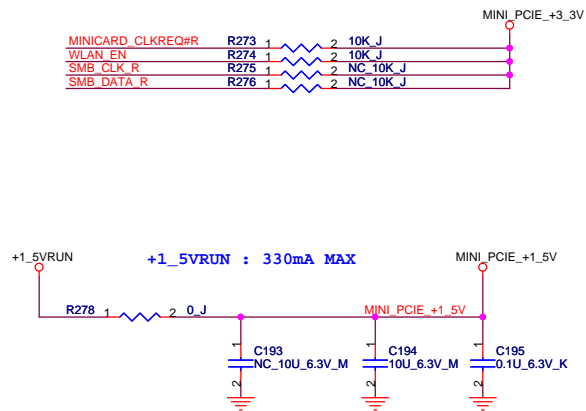


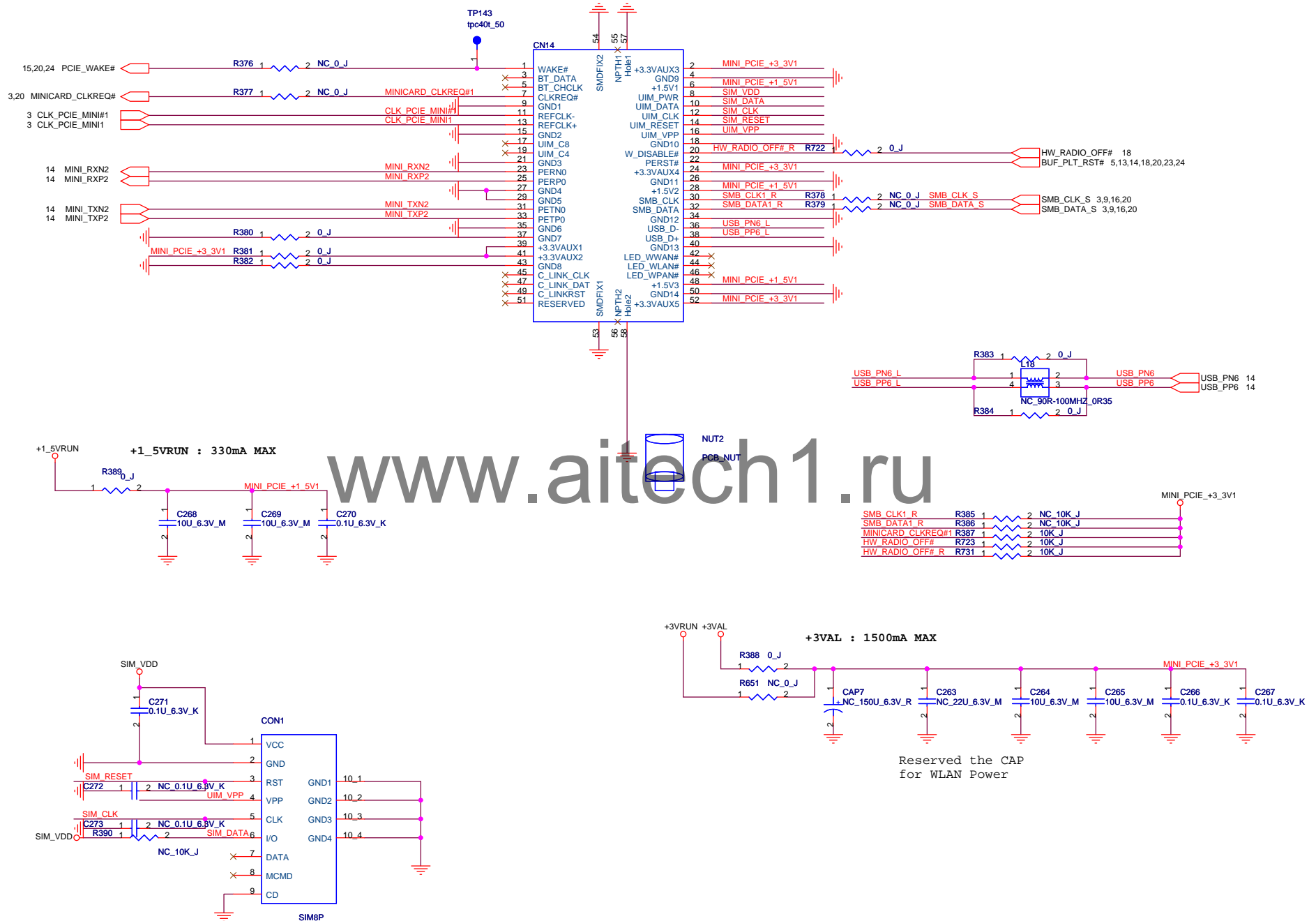






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5

4

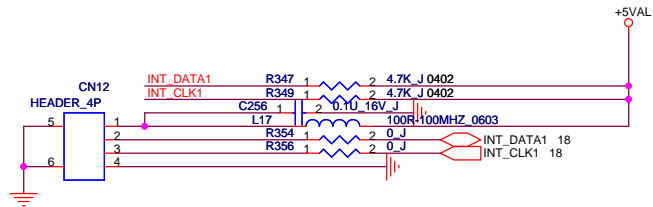
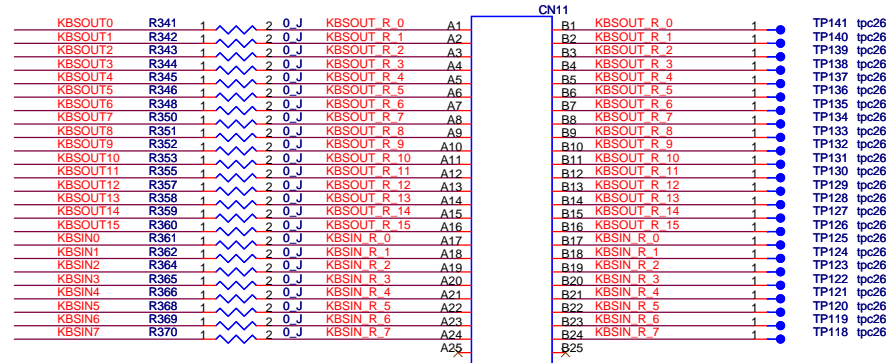
3

2

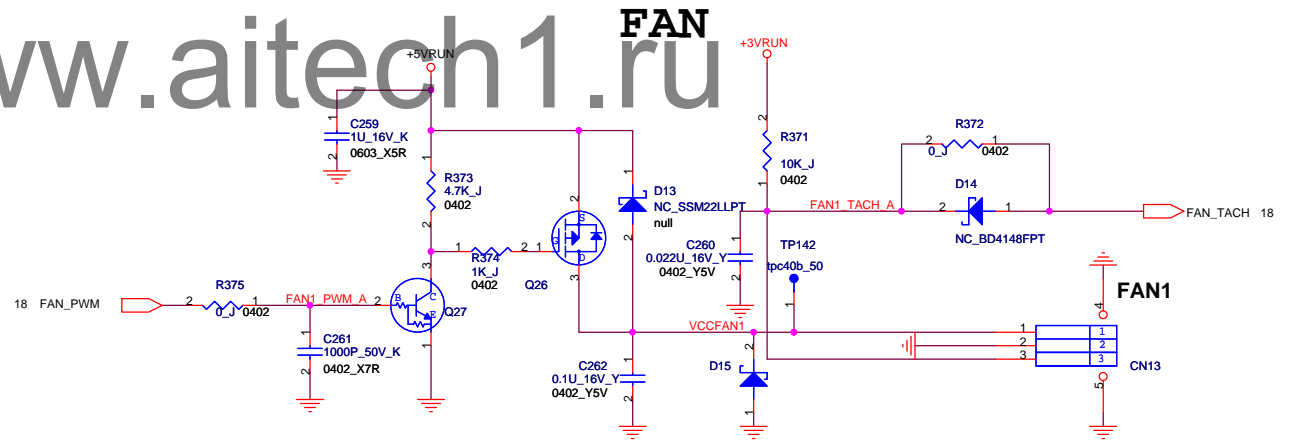
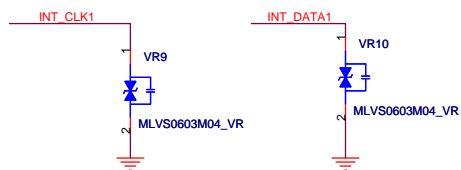
1

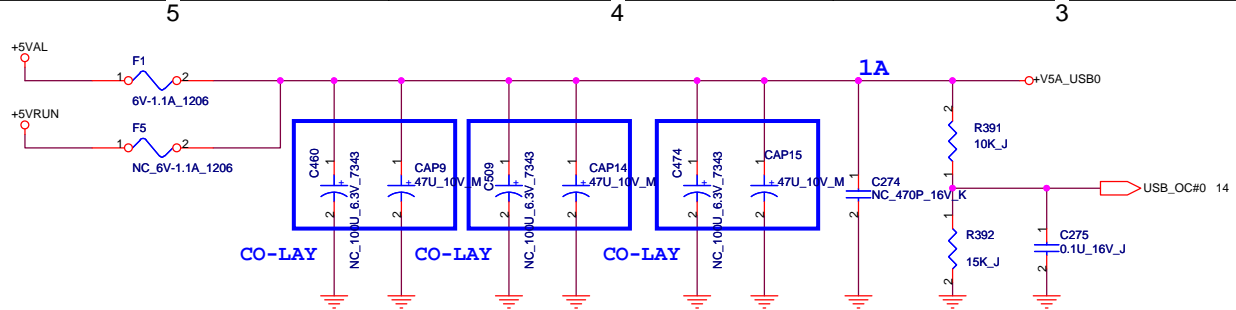
KBSOUT[0..15] 18

KBSIN[0..7] 18

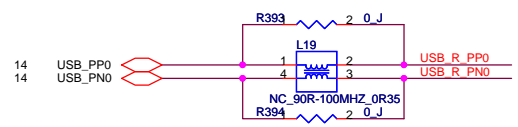
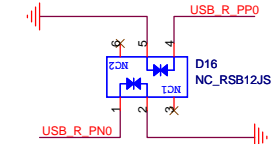
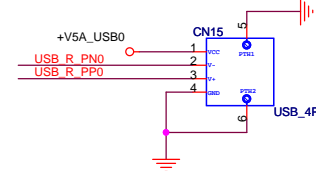


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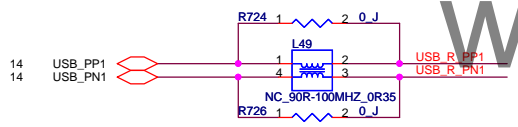
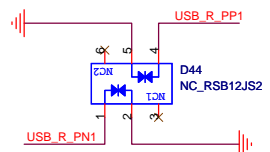
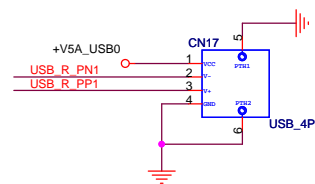




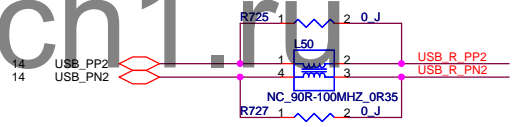
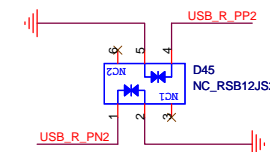
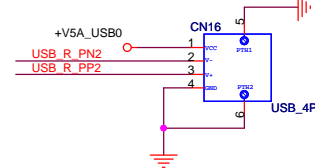
USB PORT 1



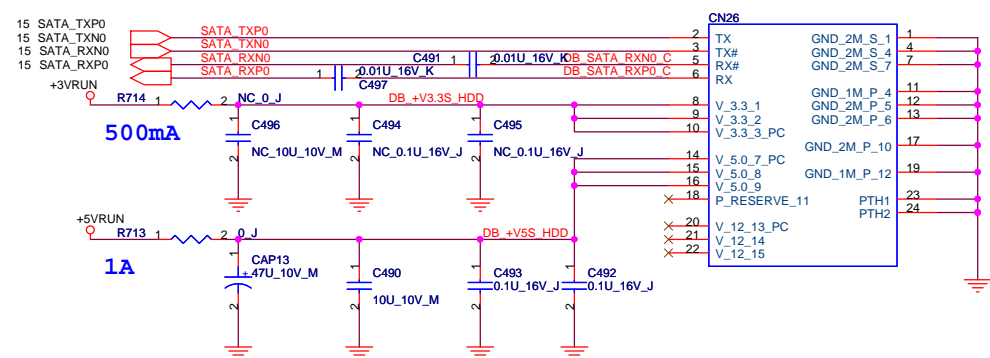
USB PORT 2



USB PORT 3



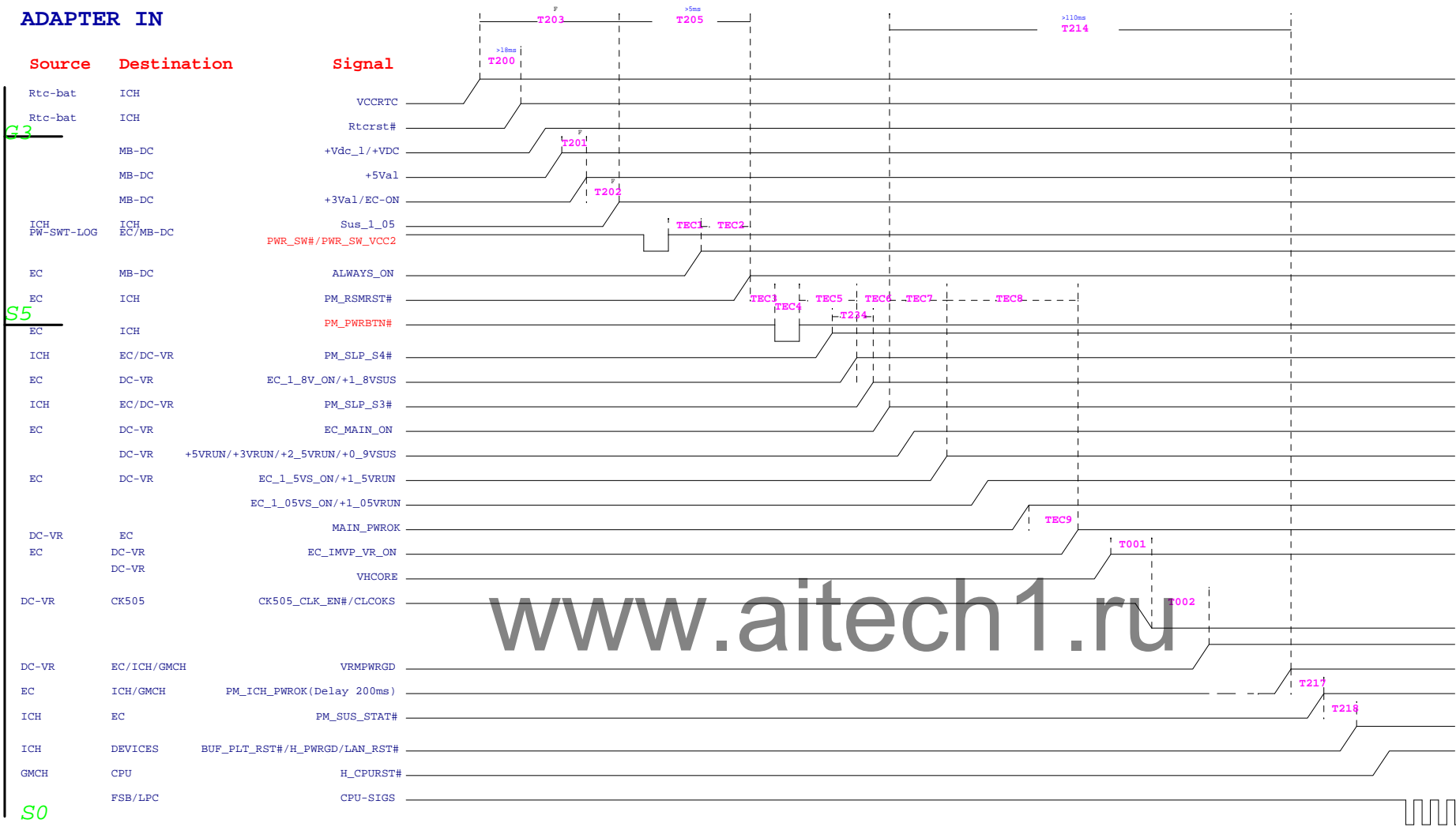
SATA HDD/SSD



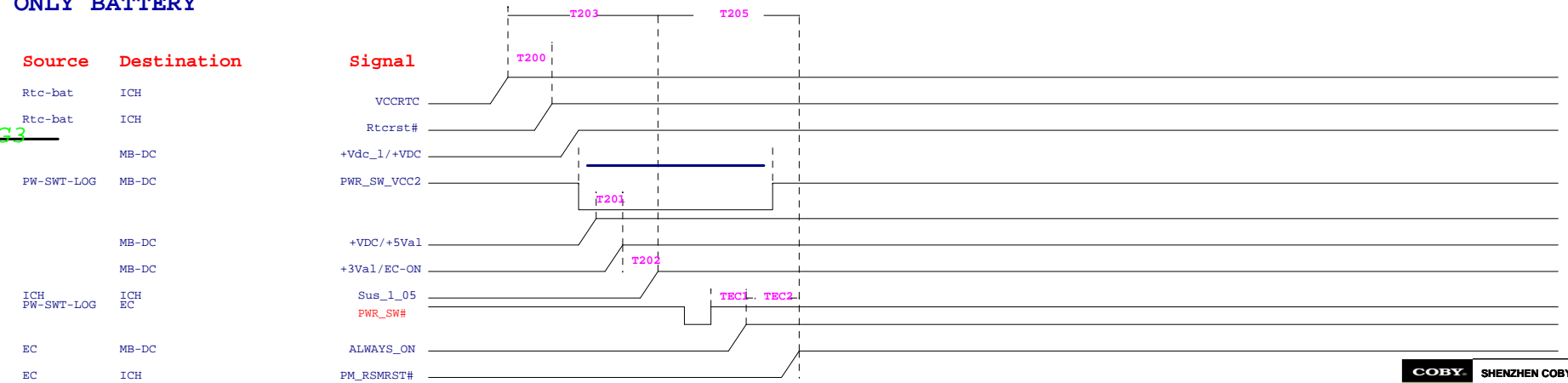
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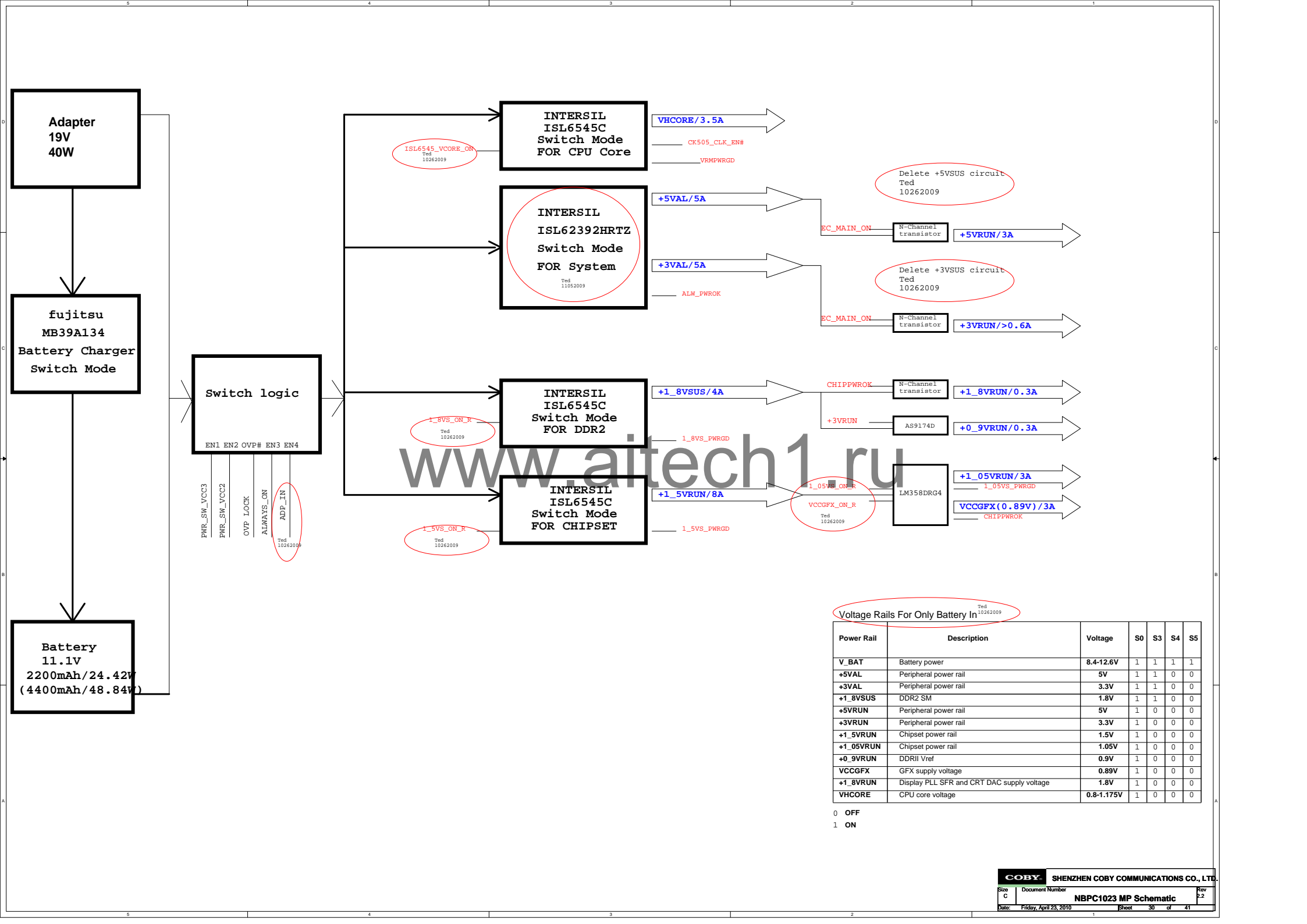
ADAPTER IN



ONLY BATTERY



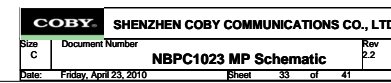
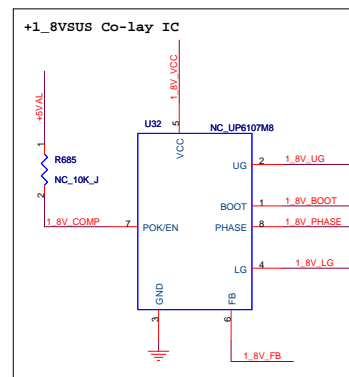
time table

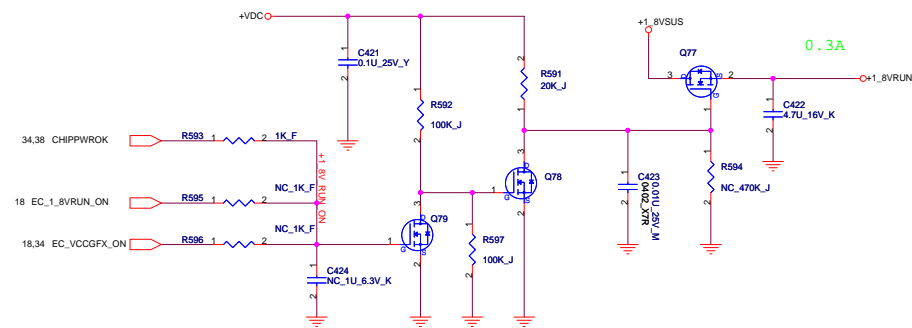
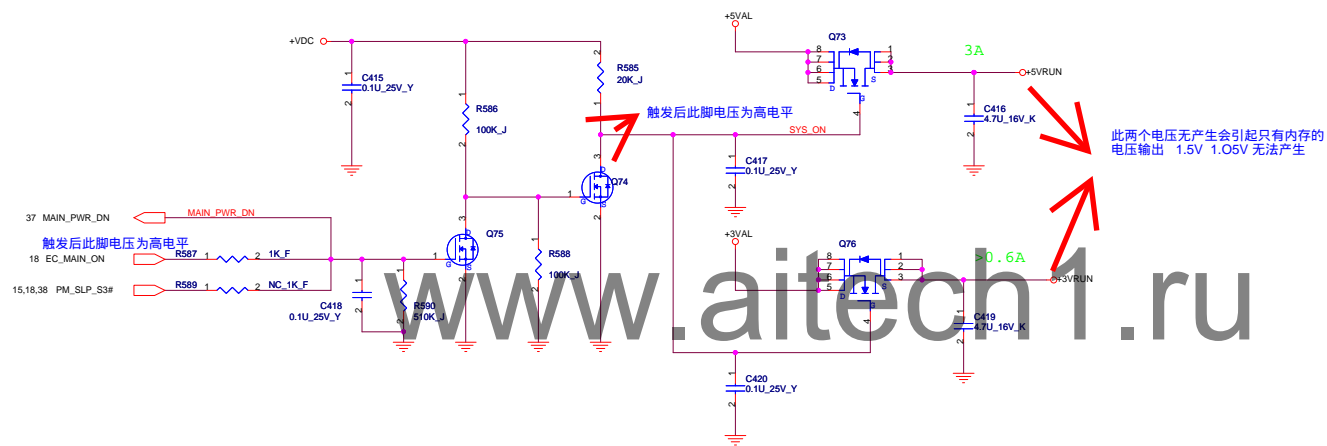


Voltage Rails For Only Battery In Ted 10262009

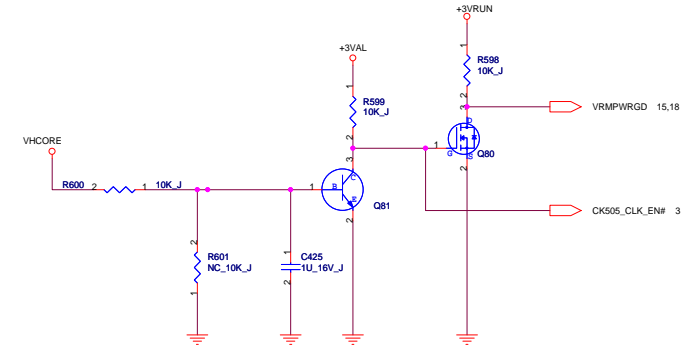
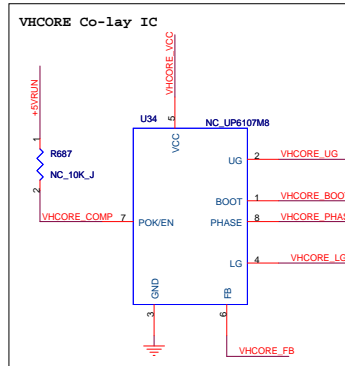
Power Rail	Description	Voltage	S0	S3	S4	S5
V_BAT	Battery power	8.4-12.6V	1	1	1	1
+5VAL	Peripheral power rail	5V	1	1	0	0
+3VAL	Peripheral power rail	3.3V	1	1	0	0
+1_8VSUS	DDR2 SM	1.8V	1	1	0	0
+5VRUN	Peripheral power rail	5V	1	0	0	0
+3VRUN	Peripheral power rail	3.3V	1	0	0	0
+1_5VRUN	Chipset power rail	1.5V	1	0	0	0
+1_05VRUN	Chipset power rail	1.05V	1	0	0	0
+0_9VRUN	DDRII Vref	0.9V	1	0	0	0
VCCGFX	GFX supply voltage	0.89V	1	0	0	0
+1_8VRUN	Display PLL SFR and CRT DAC supply voltage	1.8V	1	0	0	0
VHORE	CPU core voltage	0.8-1.175V	1	0	0	0

0 OFF
1 ON

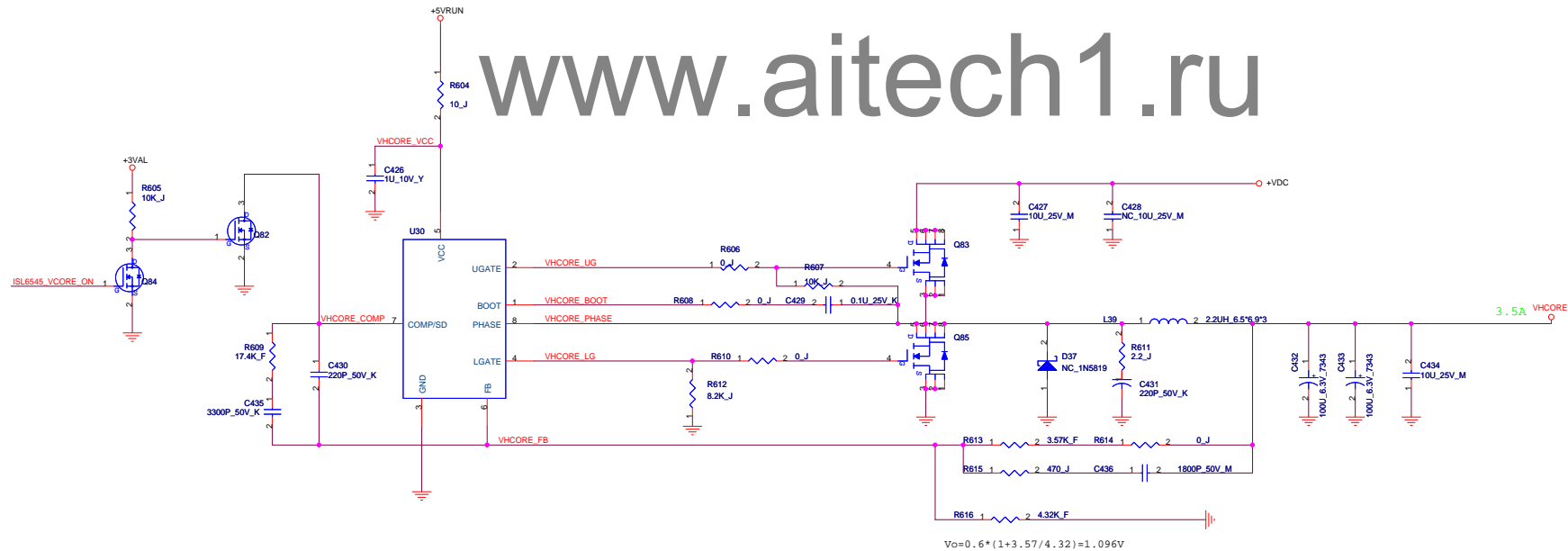


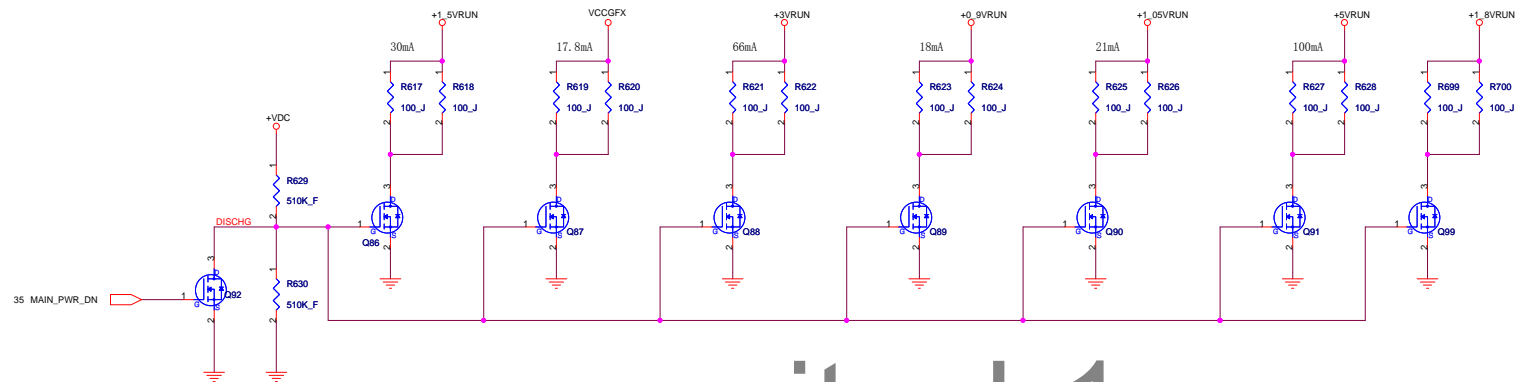


18,38 MAIN_PWROK R602 1 2 NC_0_J ISL6545_VCORE_ON
18 EC_IMVP_VR_ON R603 1 2 0_J

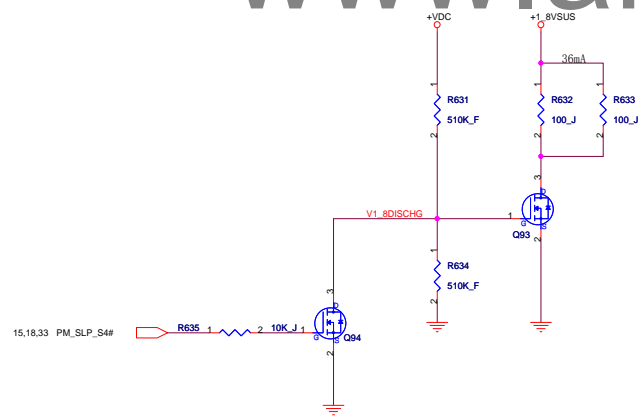


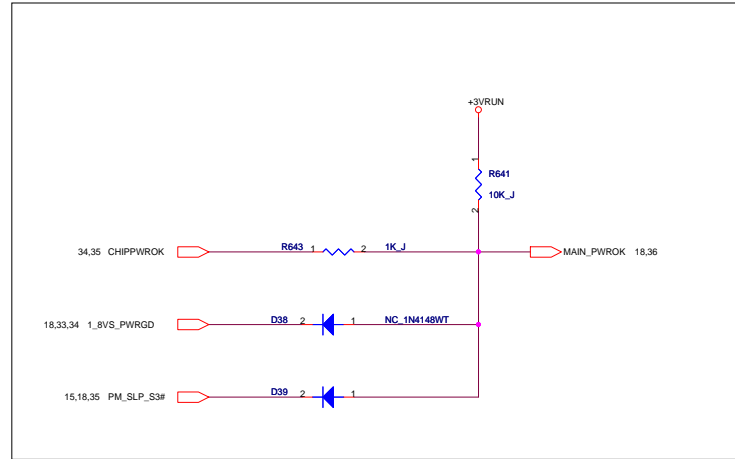
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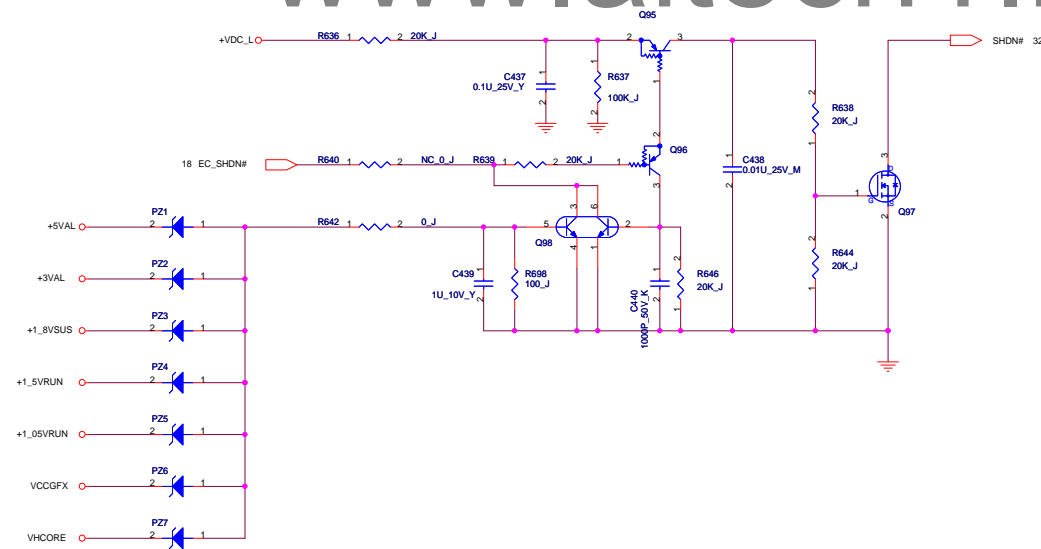


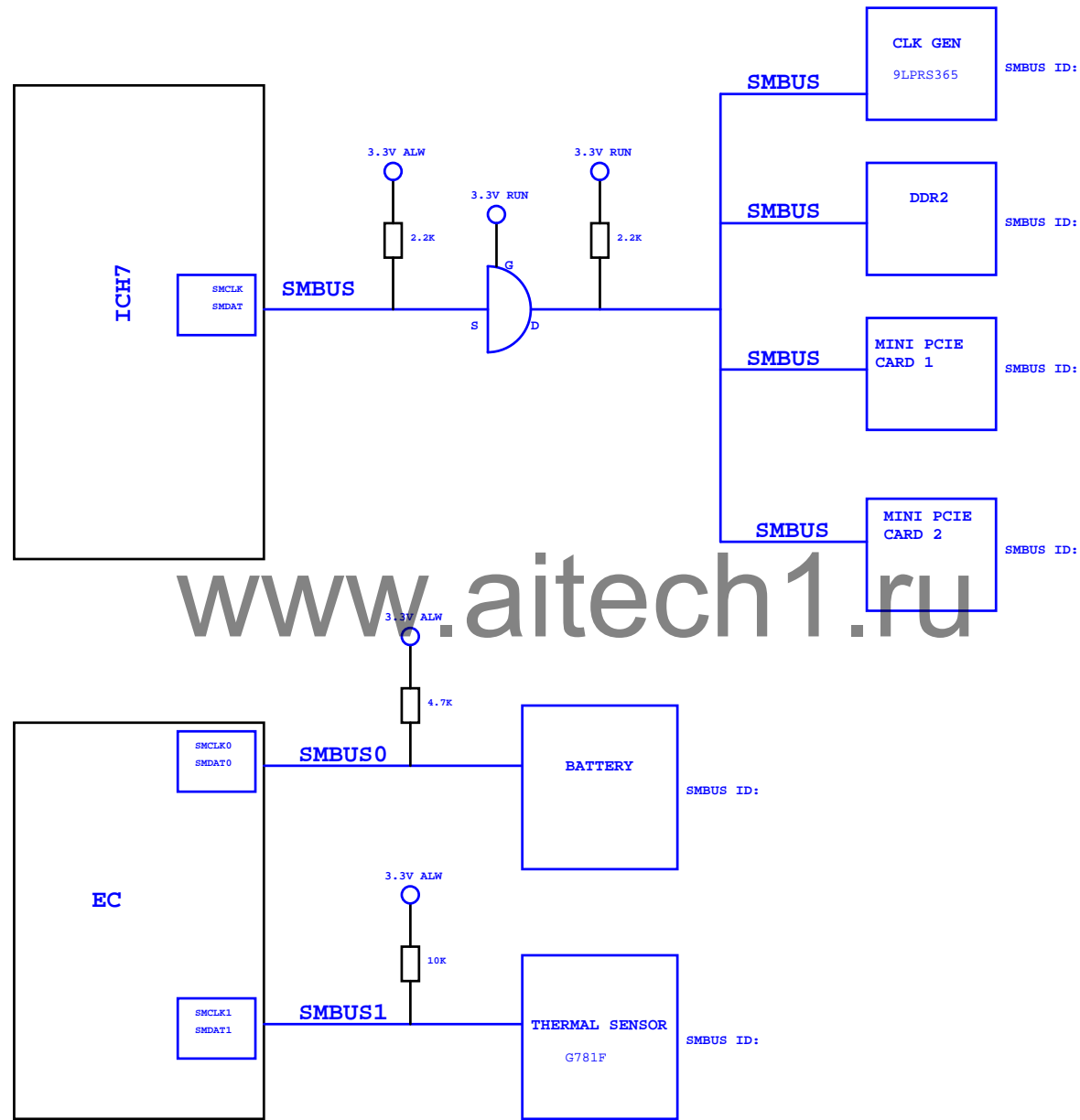
www.aitech1.ru

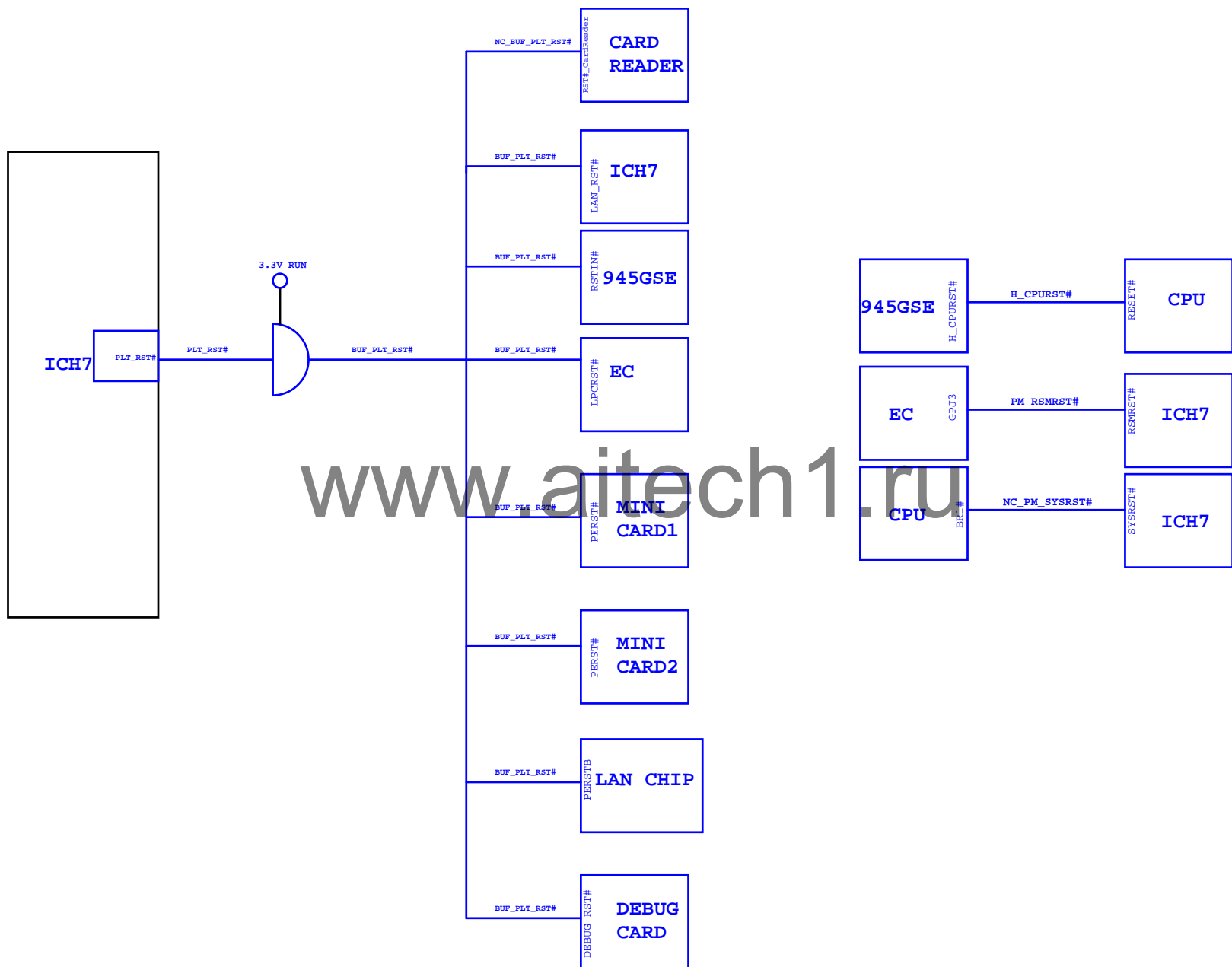




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